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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,922	06/07/2004	Ta-Chia Yeh	REAP0027USA	3921

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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,922	YEH, TA-CHIA	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Newly added claims 18-21 are pending in the current application and have been examined. Claims 1-17 have been cancelled.

2. In response to Applicant's amendment filed 06/26/2006, the Examiner has withdrawn the objections to the Drawings and Specification.

3. The canceling of claims 1-17 has rendered the claim objections and 35 U.S.C. 112, first and second paragraph rejections moot.

Response to Arguments

4. Applicant's arguments with respect to claims 18-21 have been considered but are moot in view of the new ground(s) of rejection. However, the Examiner would like to respond to some aspects of the Applicant's arguments.

Applicant's Admitted Prior Art (AAPA) Fig. 1 teaches all aspects of the claimed invention **except** for the delay elements. Lurkins (US-6964002) was combined with AAPA to add the delay elements **only** to arrive at the claimed invention. The Applicant's arguments seems to be fixated on Lurkins not teaching the elements or structure of the claimed invention that it was never intended to teach. Lurkins is analogous art because it teaches the principle and structure of using delay elements to correct clock skew for different scan chains as in Fig. 3, but was not used to teach the structure as in Fig. 1 as Applicant's argument purports. Therefore, The Examiner asserts that the claimed

invention as claimed in newly added claims 18-21 is **still** substantially taught by AAPA in view of Lurkins.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 18-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 18:

The claim limitation "a first multiplexer coupled to the first delayed test clock, and the first logic signal or the first clock signal for outputting an output signal being the first logic signal, the first clock signal or the first delayed test clock according to a control signal" fails to comply with the written description requirement because the multiplexer disclosed in the specification is only a two input multiplexer. According to Fig. 3, the multiplexer, which is coupled to the logic signal LOG1 is also only coupled to the delayed test clock TEST_CLK2 not the "first clock signal" CLK1. Therefore, the claim limitation above as written is incorrect and must be corrected in response to this office action.

Also, the claim limitation "a second multiplexer coupled to the second delayed test clock (Fig. 3, TEST_CLK4), and the second clock or the second logic signal for outputting an output signal being the second clock, the second logic signal, or the second delayed test clock according to the control signal" fails to comply with the written description requirement for the same reasons as the first multiplexer. Therefore, the claim limitation above as written is incorrect and must be corrected in response to this office action.

Claim 19:

The claim limitation "a third multiplexer coupled to the third delayed test clock (Fig. 3, TEST_CLK3) and the second clock (CLK2) or the second logic signal for outputting an output signal being the second clock, the second logic signal, or the third delayed test clock according to the control signal" fails to comply with the written description requirement because the multiplexer disclosed in the specification is only a two input multiplexer. According to Fig. 3, the multiplexer, which is coupled to the third delayed test clock and the second clock, is not coupled to the second logic signal. Therefore, the claim limitation above as written is incorrect and must be corrected in response to this office action.

Claims 20-21:

These claims are also rejected because they depend on claim 18 and have the same problems of failing to comply with the written description requirement.

The following is a quotation of the **second paragraph** of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 20:

This claim recites the limitation "the first element" in line 3. There is insufficient antecedent basis for this limitation in the claim. This should recite "the first delay element".

This claim recites the limitation "the second element" in line 4. There is insufficient antecedent basis for this limitation in the claim. This should recite "the second delay element".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art, hereinafter AAPA, in view of Lurkins (US-6964002), hereinafter Lurkins.

Claim 18:

AAPA teaches a first clock domain (**Fig. 1, 110**) for doing logic operations (**Fig. 1, 112**) according to a first clock (**Fig. 1, CLK1**) and generating a first logic signal (**Fig. 1, LOG1**). AAPA also teaches a first multiplexer (**Fig. 1, MUX 116**) coupled a *non-delayed* test clock (**Fig. 1, TEST_CLK**), and the first logic signal (**Fig. 1, LOG1**) for outputting an output signal being the first logic signal (**Fig. 1, LOG1**), or the *non-delayed* test clock (**Fig. 1, TEST_CLK**) according to a control signal (**Fig. 1, TEST_MODE**). AAPA further teaches a first flip-flop group including a plurality of flip-flops (**Fig. 1, first flip-flop group 120**) for doing a scanning test according to the output signal of the first multiplexer (**Fig. 1, MUX 116**).

AAPA goes on to teach a second clock domain (**Fig. 1, 150**) for doing logic operations (**Fig. 1, 152**) according to a second clock (**Fig. 1, CLK2**) and generating a second logic signal (**Fig. 1, LOG2**). AAPA also teaches a second multiplexer (**Fig. 1, MUX 156**) coupled to a *non-delayed* test clock (**Fig. 1, TEST_CLK**), and the second logic signal (**Fig. 1, LOG2**) for outputting an output signal being the second logic signal (**Fig. 1, LOG2**), or the second *non-delayed* test clock (**Fig. 1, TEST_CLK**) according to the control signal (**Fig. 1, TEST_MODE**). AAPA further teaches a second flip-flop group including a plurality of flip-flops (**Fig. 1, second flip-flop group 160**) for doing a scanning test according to the output signal of the second multiplexer (**Fig. 1, MUX 156**).

AAPA does not explicitly teach "a first delay element coupled to a test clock for delaying the test clock by a first delay time to thereby generate a first delayed test

clock", "a second delay element coupled to the test clock for delaying the test clock by a second delay time to thereby generate a second delayed test clock" and the coupling of the first and second delay elements to the first and second multiplexers to generate first and second delayed test clocks. However, AAPA does teach a *non-delayed* test clock coupled to the first and second multiplexers.

Lurkins teaches in an analogous art a base clock signal enters the MUX 20 on connection 15 and is split into two branches 90 (**Fig. 1, LOG1**) and 92 (**Fig. 1, TEST_CLK**). Branch 90 (**Fig. 1, LOG1**) goes directly into a switch 98 (**Fig. 1, MUX 116**) while branch 92 (**Fig. 1, TEST_CLK**) enters a delaying unit 94. The delaying unit 94 can be a delay cell, an inverter, or other mechanism that retains the shape and frequency of the clock signal. Lurkins also teaches the delayed signal from the delaying unit 94 enters switch 98 (**Fig. 1, MUX 116**) via connection 96 (delayed test clock signal). Lurkins further teaches a selection line 100 (**Fig. 1, TEST_MODE**) allows a user to set switch 98 so that either the undelayed clock signal from connection 90 (**Fig. 1, LOG1**) or the delayed clock signal from connection 96 (delayed test clock signal) is placed on output 30. (Col. 5, ll. 45-58, Fig. 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify AAPA to add Lurkins' delaying unit 94 in order to delay the AAPA's TEST_CLK connection to the multiplexers 116 and 156 of Fig. 1 in order to generate the first and second delayed test clocks. The artisan would be motivated to do so because introducing Lurkins' delaying unit 94 to the AAPA's TEST_CLK will enable AAPA to reduce the chances of race conditions occurring between the different flip-flop

groups (scan chains) during scan testing mode. The artisan would also be motivated to do so because it would enable AAPA to switch between a functional clock (LOG1, LOG2) and the first and second delayed test clocks (delayed TEST_CLK outputted from Lurkins' delaying unit 94) during scan testing mode. (See Lurkins Col. 1, ll. 17-19, l. 51 to col. 2, ll. 54, col. 3, ll. 11-23).

Further the limitation "the first delay time is longer than the second delay time" would be an obvious design choice to one skilled in the art. The artisan would also be motivated to do so because Lurkins teaches delaying the second clock from the first clock up to 180 degrees from each other to prevent race conditions. (Col. 3, ll. 11-23).

Claim 19:

AAPA teaches the second clock domain (**Fig. 1, 150**) further comprises a third multiplexer (**Fig. 1, 154**) coupled to a *non-delayed* test clock (**Fig. 1, TEST_CLK**) and the second clock (**Fig. 1, CLK2**) for outputting an output signal being the second clock (**Fig. 1, CLK2**), or the *non-delayed* test clock (**Fig. 1, TEST_CLK**) according to the control signal (**Fig. 1, TEST_MODE**). AAPA also teaches a third flip-flop group (**Fig. 1, third flip-flop group 158**) including a plurality of flip-flops for doing a scanning test according to the output signal of the third multiplexer (**Fig. 1, 154**).

AAPA does not explicitly teach "a third delay element coupled to the test clock for delaying the test clock by a third delay time to thereby generate a third delayed test clock" and the coupling of the third delay elements to the third multiplexer to generate a third delayed test clock. However, AAPA does teach a *non-delayed* test clock coupled to the first and second multiplexers.

Lurkins teaches in an analogous art a base clock signal enters the MUX 20 on connection 15 and is split into two branches 90 (**Fig. 1, CLK2**, the second clock) and 92 (**Fig. 1, TEST_CLK**). Branch 90 (**Fig. 1, CLK2**, the second clock) goes directly into a switch 98 (**Fig. 1, MUX 154**) while branch 92 (**Fig. 1, TEST_CLK**) enters a delaying unit 94. The delaying unit 94 can be a delay cell, an inverter, or other mechanism that retains the shape and frequency of the clock signal. Lurkins also teaches the delayed signal from the delaying unit 94 enters switch 98 (**Fig. 1, MUX 154**) via connection 96 (delayed test clock signal). Lurkins further teaches a selection line 100 (**Fig. 1, TEST_MODE**) allows a user to set switch 98 so that either the undelayed clock signal from connection 90 (**Fig. 1, CLK2**, the second clock) or the delayed clock signal from connection 96 (delayed test clock signal) is placed on output 30. (Col. 5, ll. 45-58, Fig. 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify AAPA to add Lurkins' delaying unit 94 in order to delay the AAPA's TEST_CLK connection to multiplexer 154 of Fig. 1. The artisan would be motivated to do so because introducing Lurkins' delaying unit 94 to the AAPA's TEST_CLK will enable AAPA to reduce the chances of race conditions occurring between the different flip-flop groups (scan chains) during scan testing mode. The artisan would also be motivated to do so because it would enable AAPA to switch between undelayed clock signal from connection 90 (**Fig. 1, CLK2**, the second clock) and a delayed test clock (**delayed TEST_CLK** outputted from Lurkins' delaying unit 94)

during scan testing mode. (See Lurkins Col. 1, ll. 17-19, l. 51 to col. 2, ll. 54, col. 3, ll. 11-23).

Further the limitation "the third delay time is different than the first delay time and the second delay time" would be an obvious design choice to one skilled in the art. The artisan would also be motivated to do so because Lurkins teaches delaying the second clock from the first clock up to 180 degrees from each other to prevent race conditions. (Col. 3, ll. 11-23).

Claim 20:

AAPA teaches the first clock domain (**Fig. 1, 110**) further comprises a fourth multiplexer (**Fig. 1, 114**) coupled to the test clock (**Fig. 1, TEST_CLK**) and the first clock (**Fig. 1, CLK1**) for outputting an output signal being the first clock or the test clock according to the control signal (**Fig. 1, TEST_MODE**). AAPA also teaches a fourth flip-flop group (**Fig. 1, 118**) including a plurality of flip-flops for doing a scanning test according to the output signal of the fourth multiplexer (**Fig. 1, 114**) and the test clock (**Fig. 1, TEST_CLK**) is input to the fourth multiplexer (**Fig. 1, 114**) without delay.

Claim 21:

Lurkins teaches "the first and the second delay elements respectively comprise one or more delay units, and the number of the delay units of the first *delay* element is different from the number of the delay units of the second *delay* element" in that the delaying unit 94 can be a delay cell, an inverter, or other mechanism that retains the shape and frequency of the clock signal. Lurkins also teaches delaying the second clock

from the first clock up to 180 degrees from each other to prevent race conditions. (Col. 5, ll. 49-54).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr. 8/30/06
Examiner
Art Unit 2138

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